What Is Claimed Is:

1. A debugging system comprising:

a host system to observe and control the step-by-step execution of a debugging operation;

a target system communicatively coupled to the host system, the target system including

a debug port having a plurality of pins;

a debug port interface coupled to the debug port; and

a power management pin separate from said plurality of pins and not coupled to the debug port via the debug port interface; and

a connection to couple one of said plurality of pins to said power management pin, said connection being independent of said debug port interface.

2. The debugging system of claim 1, wherein the one of said plurality of pins is a general purpose pin and the power management pin is a system sleep pin.

3. The debugging system of claim 1, wherein the one of said plurality of pins is a general purpose pin and the power management pin is a system stopclock pin.

4. The debugging system of claim 1, wherein the one of said plurality of pins is a debug pin and the power management pin is a system error pin.

5. The debugging system of claim 1, wherein the one of said plurality of pins

is a debug pin and the power management pin is a system reset pin

6. The debugging system according to claim 1, wherein the connection is one of blue-wiring, rework, or a post-fabrication board connection.

7. A method of debugging, comprising:

sampling a power management signal on a device, the power management signal being separate from a test access port of the device;

determining whether a power management transition has occurred on the device based on the power management signal; and

triggering a debug mode if a power management transition has occurred.

8. The method according to claim 7, wherein the power management signal is a system sleep signal.

9. The method according to claim 7, said determining further comprising:

determining whether the device has entered a sleep state within which the device is capable of entering a debug mode.

10. A method of debugging, comprising:

issuing a command to halt execution on a device;

querying a sleep pin on the device to determine whether the sleep pin is asserted;

asserting a system error pin on the device to wake up the device;

querying a stopclock pin on the device to determine whether the sleep pin is de-asserted; and

processing the halt command.

11. The method according to claim 10, wherein said asserting, querying, and processing are completed only if the sleep pin is asserted.

12. The method according to claim 10, wherein the device comprises a debug port and a debug port interface and the system error pin is not coupled to the debug port via the debug port interface.

13. A method of debugging, comprising:

deferring power management transitions on a device;

issuing a test access port scan to the device; and

determining whether a power management transition occurred during the test access port scan.

14. The method according to claim 13, said deferring comprising:

clearing a first bit and a second bit in a power management register if power state transitions are not deferred;

setting the first bit and clearing the second bit if power state transitions are always deferred;

setting the first bit and clearing the second bit if a target device is in debug mode and power state transitions are deferred while the target device is in debug mode; and

clearing the first bit and setting the second bit if a target device is not in debug mode and power state transitions are deferred after a breakpoint.

15. The method according to claim 13, further comprising:

reporting to a user that a power management transition occurred during the test access port scan.

16. A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to:

observe a power management pin assertion on a device, the power management pin assertion being distinct from Joint Test Access Group (JTAG) pin assertions of the device;

determine whether a power state transition has occurred on the device based on the power management pin assertion; and

place the device in a debug mode if a power state transition has occurred.

17. The machine accessible medium according to claim 16, wherein the power management pin is a system sleep pin.

18. The machine accessible medium according to claim 16, further comprising

instructions that cause the processor to:

determine whether the device has entered a sleep state within which the device is capable of entering the debug mode prior to entering the debug mode.

19. A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to:

issue a command to halt execution of a device;

determine whether a sleep pin of the device is asserted;

assert a system error pin on the device to transition the device to an elevated sleep state;

query a stopclock pin on the device to determine whether the sleep pin is de-asserted; and

process the halt command.

20. The machine accessible medium according to claim 19, further comprising instructions to query a sleep pin on the device to determine whether the sleep pin is asserted.

21. The machine accessible medium according to claim 19, wherein the processor will assert the system error pin, query the stopclock pin, and process the halt command only if the sleep pin is asserted.

22. A machine accessible medium containing program instructions that, when

executed by a processor, cause the processor to:

receive a command that indicates to the processor how to defer power state transitions in a target device;

clear a first bit and a second bit in a designated register of a target device if the command indicates that power state transitions are not deferred;

set the first bit and clear the second bit if the command indicates that power state transitions are always deferred;

set the first bit and clear the second bit if the target device is in debug mode and the command indicates that power state transitions are deferred while the target device is in debug mode; and

clear the first bit and set the second bit if the target device is not in debug mode and the command indicates that power state transitions are deferred after a breakpoint.

23. The machine accessible medium according to claim 22, further comprising instructions to:

defer power state transitions based on the command;

issue a test access port scan to the target device; and

determine whether a power state transition occurred during the test access port scan.

24. The machine accessible medium according to claim 23, further comprising instructions that cause the processor to:

report to a user that a power state transition occurred during the test access port scan.